UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/609,690	07/05/2000	Handong Wu	252/110	4070

28875 7590 04/20/2005

Zilka-Kotab, PC
P.O. BOX 721120
SAN JOSE, CA 95172-1120

EXAMINER	
GOLD, AVI M	
ART UNIT	**PAPER NUMBER**
2157	

DATE MAILED: 04/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/609,690	WU ET AL.	
	Examiner	Art Unit	
	Avi Gold	2157	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18 and 30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18 and 30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The amendment received on September 29, 2004 has been entered and fully considered.

Response to Amendment

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-16 and 30 are rejected under 35 U.S.C. 102(e) as being anticipated by Kadambi et al., U.S. Patent No. 6,850,521.

Kadambi teaches the invention as claimed including a method and apparatus for high performance switching of data packets in local area communications networks (see abstract).

Regarding claim 1, Kadambi teaches an apparatus for processing data packets, comprising:

a first data processing unit adapted to filter incoming packets (col. 31, lines 35-45, Kadambi discloses filtering of incoming packets in the FFP);

an addressable memory unit in which a plurality of instruction sets for packet processing are stored (col. 35, lines 57-64, Kadambi discloses the storage of different actions to be done on packets);

a second data processing unit adapted to process incoming packets according to one of said plurality of instruction sets after the filtering, based on a thread assigned to the incoming packets by the first data processing unit (col. 35, lines 24-38, Kadambi discloses packets tagged for processing after filtering); and

a data bus connecting the addressable memory unit and the first and second data processing units. (fig. 14, fig. 15, Kadambi discloses a data bus connecting the units).

Regarding claim 2, Kadambi teaches the apparatus of claim 1, further comprising a policy condition table connected to said first data processing unit, said policy condition table having a plurality of rules stored therein (col. 31, lines 20-34, Kadambi discloses a rules engine attached to the FFP).

Regarding claim 3, Kadambi teaches the apparatus of claim 1, further comprising a policy action table connected to said data bus and said addressable memory unit, wherein said policy action table stores at least one data processing policy (col. 35, lines 57-64, Kadambi discloses a filtering logic).

Regarding claim 4, Kadambi teaches the apparatus of claim 3, wherein at least one of said policies comprises:

a first address pointer element for identifying the location in said addressable memory unit of one of said plurality of instruction sets (col. 35, lines 57-64, Kadambi discloses logic 1411 in the FFP 141 which points to instruction sets to take action), and

a second address pointer element for identifying the location in said addressable memory unit of a state block (col. 31, lines 20-34, Kadambi discloses the FFP which is essentially a state machine).

Regarding claim 5, Kadambi teaches the apparatus of claim 3, wherein said first data processing unit assigns a thread to each said incoming packet, wherein said thread corresponds to one of said policies stored in said policy action table (col. 35, lines 24-65).

Regarding claim 6, Kadambi teaches the apparatus of claim 3, wherein said first data processing unit comprises logic for matching a first incoming packet to a stored first rule and for generating a first thread if the first incoming packet matches said first rule, said first thread identifying the location of one of said at least one data processing policies in said policy action table (col. 35, lines 24-65).

Regarding claim 7, Kadambi teaches the apparatus of claim 6, wherein said second data processing unit is adapted to process the first incoming packet according to said data processing policy corresponding to said first thread (col. 31, lines 20-34, col. 35, lines 24-65, Kadambi discloses the use of FIFO in the FFP).

Regarding claim 8, Kadambi teaches the apparatus of claim 6, wherein said data processing policy comprises a first address pointer to a starting address of a first set of instructions and a second address pointer to a starting address of a state block stored in said addressable memory unit, said state block used by said first set of instructions for processing the first incoming packet (col. 31, lines 20-34, col. 35, lines 57-64).

Regarding claim 9, Kadambi teaches the apparatus of claim 6, wherein said thread is assigned to said first incoming packet based on said first rule (col. 30, lines 54-61, col. 35, lines 24-65).

Regarding claim 10, Kadambi teaches the apparatus of claim 6, wherein said first processing unit further comprises logic for matching a second incoming packet to a stored second rule and for generating a second thread if the second incoming packet matches the second rule, said second thread identifying the location of one of said at least one data processing policy in said policy action table (col. 35, lines 24-65, Kadambi discloses different rules used in the filtering logic).

Regarding claim 11, Kadambi teaches the apparatus of claim 10, wherein said second data processing unit is adapted to process the second incoming packet according to said data processing policy corresponding to said second thread (col. 35, lines 24-65).

Regarding claim 12, Kadambi teaches the apparatus of claim 10, wherein said second thread is assigned to said second incoming packet based on said second rule (col. 35, lines 24-65).

Regarding claim 13, Kadambi teaches the apparatus of claim 3, wherein said first processing unit further comprises logic for matching a plurality of incoming packets to a stored corresponding plurality of rules and for generating a thread for each packet that matches one of said plurality of rules, each said thread identifying the location of one of said at least one data processing policy in said policy action table (col. 35, lines 24-65).

Regarding claim 14, Kadambi teaches the apparatus of claim 13, wherein the second data processing unit is adapted to process each packet according to said data processing policy corresponding to said thread associated with said packet (col. 35, lines 24-65).

Regarding claim 15, Kadambi teaches the apparatus of claim 13, further comprising a memory unit connected to said first data processing unit and to said second data processing unit, said memory unit adapted to temporarily store packets before processing by said second data processing unit (col. 31, lines 35-45, col. 35, lines 24-65, Kadambi discloses packets stored within FFP).

Regarding claim 16, Kadambi teaches the apparatus of claim 1, wherein said second data processing unit comprising a plurality of general purpose processors for executing instructions in parallel (col. 5, lines 46-54, Kadambi discloses a plurality of modular systems on chip for parallel processing)

Regarding claim 30, Kadambi teaches an apparatus for processing data packets, comprising:

a first data processing unit adapted to filter incoming packets (col. 31, lines 35-45);

an addressable memory unit in which a plurality of instruction sets for packet processing are stored (col. 35, lines 57-64);

a second data processing unit adapted to process incoming packets according to one of said plurality of instruction sets after the filtering, based on a thread assigned to the incoming packets by the first data processing unit (col. 35, lines 24-38);

a data bus connecting the addressable memory unit and the first and second data processing units (fig. 14, fig. 15);

wherein a policy condition table connected to said first data processing unit, said policy condition table having a plurality of rules stored therein (col. 31, lines 20-34);

wherein a policy action table connected to said data bus and said addressable memory unit, wherein said policy action table stores at least one data processing policy (col. 35, lines 57-64);

wherein said first data processing unit comprises logic for matching a first incoming packet to a stored first rule and for generating a first thread if the first incoming packet matches said first rule, said first thread identifying the location of one of said at least one data processing policies in said policy action table (col. 35, lines 24-65);

wherein said second data processing unit is adapted to process the first incoming packet according to said data processing policy corresponding to said first thread (col. 30, lines 54-61, col. 35, lines 24-65);

wherein said data processing policy comprises a first address pointer to a starting address of a first set of instructions and a second address pointer to a starting address of a state block stored in said addressable memory unit, said state block used by said first set of instructions for processing the first incoming packet (col. 31, lines 20-34, col. 35, lines 57-64);

wherein said first processing unit further comprises logic for matching a second incoming packet to a stored second rule and for generating a second thread if the second incoming packet matches the second rule, said second thread identifying the location of one of said at least one data processing policy in said policy action table;

wherein said second data processing unit is adapted to process the second incoming packet according to said data processing policy corresponding to said second thread (col. 35, lines 24-65);

wherein a memory unit connected to said first data processing unit and to said second data processing unit, said memory unit adapted to temporarily store packets before processing by said second data processing unit (col. 5, lines 46-54);

wherein said second data processing unit comprising a plurality of general purpose processors for executing instructions in parallel (col. 5, lines 46-54);

wherein the apparatus includes a control logic unit coupled to an input and the policy condition table for feeding an arithmetic logic unit, which is in turn coupled to the policy action table and the state block for generating an output (col. 31, lines 35-45, col. 35, lines 24-65)

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kadambi in view of Scales, U.S. Patent No. 5,761,729.

Kadambi teaches the invention substantially as claimed including a method and apparatus for high performance switching of data packets in local area communications networks (see abstract).

As to claim 17, Kadambi teaches the method of claim 16.

Kadambi fails to teach the limitation further including at least one said general purpose processor comprising a complex instruction set computer processor.

However, Scales teaches a distributed computer system including a distributed shared memory (see abstract). Scales shows evidence of the use of a complex

instruction set computer processor (col. 1, lines 63-67; col. 2, lines 1-7, 49-67; col. 3, lines 1-8, 41-63).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Kadambi in view of Scales to use a complex instruction set computer processor. One would be motivated to do so because a complex instruction set processor can perform several low-level operations and can deal with packet complexity.

As to claim 18, Kadambi teaches the method of claim 16.

Kadambi fails to teach the limitation further including at least one said general purpose processor comprising a reduced instruction set computer processor.

However, Scales teaches a distributed computer system including a distributed shared memory (see abstract). Scales shows evidence of the use of a reduced instruction set computer processor (col. 1, lines 63-67; col. 2, lines 1-7, 49-67; col. 3, lines 1-8, 41-63).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Kadambi in view of Scales to use a reduced instruction set computer processor. One would be motivated to do so because a reduced instruction set processor allows for rapid execution of a sequence of simple instructions.

Response to Arguments

5. In view of the appeal brief filed on September 29, 2004, PROSECUTION IS HEREBY REOPENED. New grounds of rejection are set forth above.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Pat. No. 5,615,340 to Dai et al.

U.S. Pat. No. 6,647,418 to Maria et al.

U.S. Pat. No. 6,493,752 to Lee et al.

U.S. Pat. No. 6,253,321 to Nikander et al.

U.S. Pat. No. 6,262,776 to Griffits.

U.S. Pat. No. 6,675,218 to Mahler et al.

U.S. Pat. No. 5,983,270 to Abraham et al.

U.S. Pat. No. 5,627,829 to Gleeson et al.

U.S. Pat. No. 6,069,827 to Sinclair

U.S. Pat. No. 6,065,065 to Murakami et al.

U.S. Pat. No. 6,167,445 to Gai et al.

U.S. Pat. No. 6,772,347 to Xie et al.

U.S. Pat. No. 6,675,218 to Mahler et al.

U.S. Pat. No. 6,647,418 to Maria et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Avi Gold whose telephone number is 571-272-4002. The examiner can normally be reached on M-F 8:00-5:30 (1st Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ario Etienne can be reached on 571-272-4001. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Avi Gold

Patent Examiner

Art Unit 2157

AMG

ARIO ETIENNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100